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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,611	07/07/2005	Satoshi Yamanaka	0925-0220PUS1	8340

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EXAMINER	
ZHU, RICHARD Z	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
12/30/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/541,611	YAMANAKA ET AL.	
	Examiner	Art Unit	
	RICHARD Z. ZHU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Acknowledgement is made of applicant's amendment made on 11/13/2009. Applicant's submission filed has been entered and made of record.

Status of the Claims

2. Claims 1-7 are pending.

Response to Applicant's Arguments

3. In light of applicant's amendment and accompanying arguments, previous grounds of rejections are vacated. Upon further search, new grounds of rejections are entered in the instant action.

4. **In response to "**on the assumption that said normal pixels are lost using said different interpolation method**".**

In a method or apparatus claim, a limitation is given patentable weight if said limitation further limit a claim element to recite a specific step within a method or structure within an apparatus. Here, if the assumption that said normal pixels are lost using said different interpolation method is to be given patentable weight, said assumption has to affect the manner in which test interpolation data is calculated in a way that distinguishes over any prior art method of calculation. If it does not, it is not given patentable weight because it does not further limit the step of test interpolation data calculation.

While the examiner has found support for said assumption within the specification, however, the specification does not articulate how such assumption affects the manner in which interpolation data are calculated that is different from prior art of record to be apply in the instant office action. Therefore, the assumption is treated as a statement of intent or reasoning for performing the limiting step of interpolation calculation. Thus, the reasoning or assumption has no patentable weight because there can be many reasons to perform a certain limiting step, but if the reasoning does not alter the resulting step in a particular manner to distinguish over a prior art step, then there is no novelty in performing said step. See *In re Wiseman, 596 F.2d at 1022, 201 USPQ at 661*, MPEP 2141.02.

If the specification contain support where such assumption does indeed affect the manner in which test interpolation data are calculated that is different from the prior art, applicant is recommended to further amend the limitation to reflect such difference.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6 are rejected under 35 USC 103(a) as being unpatentable over ***Ashibe et al. (JP 363122385 A)*** in view of ***Jiang (US 7242819 B2)***.

A full translation for ***Ashibe*** will be available for the next office action. In the instant action, drawings and English abstract of ***Ashibe*** is relied upon.

Regarding the apparatus of Claim 1 and therefore method of Claim 4, ***Ashibe*** discloses a pixel interpolation circuit (**Drawing 2, Unit 20**) for generating interpolation pixel data which interpolates an input image based on pixel data composing the input image (**See Abstract**), the pixel interpolation circuit comprising:

an interpolation unit (**Drawing 2, Unit 20**) for calculating interpolation candidate data of the same interpolation pixel based on calculations performed on test interpolation data of a plurality of normal pixels neighboring the interpolation pixel (**Drawing 3, "o" are normal pixels neighboring interpolation pixels "x", see Abstract "initially, interpolation to respective modes are carried out". Particularly 3(c) where "x" is interpolated using neighboring "o"**), where each interpolation candidate data is to be interpolated using different interpolation methods (**Abstract, "the four types of thinning out and interpolating methods shown in the drawings (a)-(d)", see Drawing 3**), wherein said test interpolation data is calculated for each of said normal pixels on the assumption that said normal pixels are lost using said different interpolation methods (**Abstract , "Then, the sum in the block of the absolute value of the difference between an interpolation signal and an original signal, namely, the quantity of the distortion to the respective modes for every block is calculates the decide the mode to all the blocks based thereon. The picture elements of the input picture signal are thinned out for every block according to the decided mode". Here, an interpolation signal for respective modes of interpolations are calculated to be compare to the original pixel value to decide which mode of interpolation to use for picture elements in every block. Why interpolate the picture elements in every block if they are not assumed to be lost?**);

a determining circuit (**Drawing 2, Unit 20**) for selecting one of the interpolation methods based on a difference between the test interpolation data and actual pixel data of said plurality of normal pixels (**Abstract, "Then, the sum in the block of the absolute value of the difference between an interpolation signal and an original signal, namely, the quantity of the distortion to the respective modes for every block is calculates the decide the mode to all the blocks based thereon"**); and

an output circuit for outputting the interpolation candidate data calculated by the selected interpolation circuit as the interpolation pixel data (**Drawing 2, Unit 20**).

While the interpolation unit of ***Ashibe*** independently calculates interpolation candidate data of the same interpolation pixel using respective different interpolation methods, ***Ashibe*** does not disclose the internal structure of said unit comprise a plurality of independent interpolation circuits.

Jiang discloses an interpolation circuitry configuration that takes edge direction into consideration when performing interpolation (**See Figs 1-2**) having an internal structure comprising a plurality of interpolation circuits with specific logic components each independently calculates interpolation candidate data (**Fig 8, Adder Logic 88 and Division Logic 90**) of a same pixel to be interpolated (**Fig 1, Pixel to be interpolated**), using different interpolation methods (**Col 13, Rows 48-58**).

Jiang demonstrated that it is well known in the art to implement separate sets of logic to form independent circuits to each perform its respective interpolation methods, it would've been obvious to one of ordinary skill in the art at the time of the invention to design the internal circuitry of interpolation unit of ***Ashibe*** with independent circuits to calculate

respective correlation values of respective different interpolation methods such that its intended function as disclosed would be successfully implemented.

Regarding Claims 2 and 5, ***Ashibe*** discloses wherein the determining circuit calculates a evaluation data for each of the interpolation circuits, by summing up the absolute values of the difference between the test interpolation data and the actual pixel data, and selects one of the interpolation circuits based on the evaluation data (**Abstract, "Then, the sum in the block of the absolute value of the difference between an interpolation signal and an original signal, namely, the quantity of the distortion to the respective modes for every block is calculates the decide the mode to all the blocks based thereon"**).

Regarding Claims 3 and 6, ***Ashibe*** discloses wherein the determining circuit calculates binarized or ternarized values of the difference between the test interpolation data and the actual pixel data (**Drawing 3 (c), at least two or more sets of neighboring "o" are used to calculate a specific "x"**).

7. Claim 7 is rejected under 35 USC 103(a) as being unpatentable over ***Ashibe et al. (JP 363122385 A)*** and ***Jiang (US 7242819 B2)*** in view of ***Utagawa (US 6563538 B1)***.

Regarding Claim 7, ***Maenaka*** does not disclose a scanner employing said interpolation circuits. ***Utagawa*** discloses an image scanner comprising an image scanner comprising a pixel interpolation circuit (**Fig 2 and see Col 5, Rows 32-40**).

Since it is well known in the art that scanner employs interpolation circuits, it would've been obvious to one of ordinary skill in the art at the time of the invention to

implement ***Maenaka***'s circuit for ***Utagawa***'s scanner such that edge pixels can be properly interpolated in view of the advantages offered by ***Maenaka***.

Conclusion

8. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Richard Z. Zhu whose telephone number is 571-270-1587 or examiner's supervisor King Y. Poon whose telephone number is 571-272-7440. Examiner Richard Zhu can normally be reached on Monday through Thursday, 6:30 - 5:00.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RZ[2]
12/21/2009

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